REMARKS

These remarks and the accompanying amendments are responsive to the Office Action mailed March 2, 2007, having a shortened statutory period for response that expires June 4, 2007. At the time of the last examination Claims 1-17 and 20-28 were pending. Claims 18, 19, 29 and 30 have been withdrawn from consideration due to a prior restriction requirement, and are herein formally cancelled.

The claims are amended herein to overcome the claim objections and 35 U.S.C. 112 rejections mentioned in sections 3-5 of the Office Action.

As a preliminary matter, section 11 of the Office Action indicated that Claims 1-17 are allowed. Accordingly, the only remaining claims at issue are Claims 20-28. Of these remaining claims, Claims 20 and 28 are independent and are amended herein. Claim 24 is cancelled, and Claims 21-23 and 25-27 depend, directly or indirectly, from Claim 20.

Sections 6 and 7 of the Office Action reject Claims 20-28 under 35 U.S.C. 102(b) as being anticipated by United States patent number 6,452,431 issued to Waldrop (the patent hereinafter referred to simply as "Waldrop"). In addition, Section 8 of the Office Action rejects Claims 20 and 28 under 35 U.S.C. 102(b) as being anticipated by United States patent number 6,337,590 issued to Millar (the patent hereinafter referred to as "Millar"). Finally, Section 10 of the Office Action rejects Claims 20-28 under 35 U.S.C. 102(e) as being anticipated by United States patent publication number 2003/0215040 applied for by Bell et al. (the publication hereinafter referred to as "Bell"). The applicants respectfully request reconsideration of each of these rejections in light of the following remarks.

Claim 20 recites *inter alia* a method for use in a delay locked loop circuit that includes a delay line and a phase detector circuit. The delay line receives a clock signal and passes the

clock signal through an adjustable number of delay elements. The phase detector circuit samples the phase of a clock signal as it exists prior to entry into the delay line and as it exists after it exits the delay line. The phase detector circuit generates one signal if the two clock signals are out of phase in one direction, and another signal if the two clock signals are out of phase in the other direction.

If the scope of the claim were this broad, then this would recite a prior art delay locked loop circuit. In fact, each of Waldrop, Millar, and Bell teach a delay locked loop circuit that has this structure. For instance, Waldrop teaches a DLL 101 that includes a phase detector 116 that generates one signal SR if the clock signals XCLK and CLKfb are out of phase in one direction, and another signal SL if the clock signals XCLK and CLKfb are out of phase in another direction. Bell teaches a DLL 100 that includes a phase detector 304 that generates one signal SL if the clock signals XCLK and CLKFB are out of phase in one direction, and another signal SR if the clock signals XCLK and CLKFB are out of phase in the other direction. Finally, Millar teaches a DLL (see Figure 3) that includes a phase detector 25 that generates out signal UP if the clock signals CLKI and CLKR are out of phase in one direction, and another signal DOWN if the clock signals CLKI and CLKR are out of phase in another direction.

However, Claim 20 recites further features, that are not taught or suggested by any of the art of record. Specifically, in the environment of such a DLL, Claim 20 recites a method in which even if the phase detector is generating a signal that is not indicative of synchronization, a filter does not necessarily adjust the number of delay elements in the delay line. Rather, the filter allows the adjustment if there have been a predetermined number of multiple consecutive signals from the phase detector that indicate a lack of synchronization. Each of the cited art will now be addressed to illustrate why this recited feature is not anticipated by the cited art.

In Walthrop, the phase detector 116 generates signals SR and SL. The shift register 108 does not do any filtering of such signals at all. Rather the shift register 108 is responsible for simply implementing the SR and SL signals to thereby directly adjust the number of adjustable delay elements in the delay line 102. For example, "[s]hift register receives the SR or the SL signal and performs a shift right or a shift left operation to select one of the taps 105A-N" (Walthrop, Col. 3, lines 10-12). The shift register 108 does not await multiple predetermined numbers of consecutive SR signals prior to implementing a shift right, nor does the shift register await multiple predetermined numbers of consecutive SL signals prior to implementing a shift left. Accordingly, Claim 20 is not anticipated by Walthrop.

In Bell, the phase detector 304 generates signals SL and SR. The adjusting circuit 306 also performs the adjustment of delay elements in the delay line 112 directly in response to an SL or SR signal, and does not await a predetermined multiple number of such signals prior to making such an adjustment. For example, "the SR or SL signal allows the adjusting unit 306 to perform a shifting operation for selecting one of the tap lines 115.1-115.n to adjust a delay of delay line 112" (Bell, paragraph 0031, part of third sentence). Once again, the adjustment unit 306 does not appear at all to await multiple instances of the SR signal prior to making an adjustment in the delay line, or multiple instances of the SL signal prior to making another adjustment in the delay line. Accordingly, Claim 20 is not anticipated by Bell.

In Millar, the phase detector 25 generates signals UP and DOWN. Here, however, the DLL also include a clock jitter filter 29. Although this filter 29 does serve to control jitter in the operation of the control circuitry when adjusting the number of adjustable elements in the delay line 13, the filter 29 does not control jitter in the same manner recited in Claim 20. Figure 5 is demonstrative of the operation of the filter 29. The filter 29 does not operate on the premise of a

predetermined numbers of UP or DOWN signals received from the phase detector 25. Rather, the filter 29 operates based on the position of the reference clock signal CLKR within a phase detection region of the CLKI signal.

Figure 5 is demonstrative of the operation of the phase detector 25 and filter 29 (see Millar, Col. 5, lines 41 through Col. 6, line 44). An example reference clock signal is presented as signal CLKR (Reference) in Figure 5. An initial state of the clock signal CLKI is represented by signal CLKI (Initial). Without the jitter control of filter 29, the object of the DLL would be simply to place the rising edge of the CLKR signal within the phase detection region of the CLKI signal. Accordingly, the control circuit would incrementally shift the number of adjustable elements in the delay line 13 until the CLKI signal achieves the state illustrated as CLKI (Early) in Figure 5. Without the filter 29, the DLL would then enter closed-loop mode.

However, with the filter 29, the DLL moves the rising edge of the CLKI signal to be closer to the rising edge of the CLKR signal, and indeed makes it so that the rising edge of the CLKI signal leads the rising edge of the CLKR signal. The filter 29 only then allows the DLL to enter closed-loop in this state in which the target rising edge of the CLKR signal is well within the phase detection region. This would reduce jitter. However, there is no inkling in Millar as to any connection between this method of jitter reduction, and a method based on counting a predetermined number of multiple consecutive UP or DOWN signals. Claim 20 simply recites a different paradigm for jitter reduction altogether. Accordingly, Claim 20 is also not anticipated by Millar.

Claim 28 is similar to Claim 20, except that Claim 28 recites a circuit that is configured to perform a method, rather than a method performed in the context of the circuit. Accordingly, Claim 28 is likewise not anticipated by any of the cited art.

Accordingly, prompt favorable action is respectfully requested. In the event that the Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, the Examiner is requested to contact the undersigned attorney.

Dated this 22nd day of August, 2007.

Respectfully submitted,

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